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10/824,489

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Frederic Reblewski

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EXAMINER

SAXENA, AKASH

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/824,489	<b>Applicant(s)</b> REBLEWSKI, FREDERIC	
	<b>Examiner</b> AKASH SAXENA	<b>Art Unit</b> 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on 03 April 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

1. Claim(s) 1-10 has/have been presented for examination based on amendment filed on 03 April 2008.
2. Claim(s) 1, 2, 4, 8-10 is/are amended.
3. previously cancelled.
4. Claim(s) 1-2 and 4-10 are rejected under 35 USC § 102.
5. Claim(s) 3 is rejected under 35 USC § 103.
6. The arguments submitted by the applicant have been fully considered. Claims 1-10 remain rejected and this action is made FINAL. The examiner's response is as follows.

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***Response to Applicant's Remarks & Examiner's Withdrawals***

**(Argument 1)** Applicant has argued in Remarks Pg.6-7:

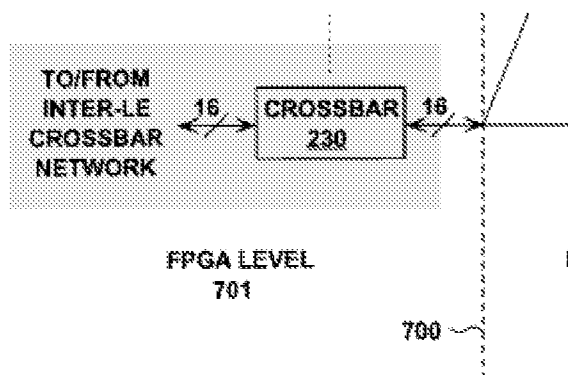
However, Barbier does not teach or suggest that each of a plurality of crossbars 631 has inputs only from one of the corresponding crossbars 230 on the left side of Fig. 7. Thus, Barbier does not teach or suggest the plurality of second reconfigurable stages each having a plurality of inputs coupled to the outputs from only the corresponding first reconfigurable interconnect stage, as now claimed. For at least this reason, it is submitted that amended claim 1 is allowable over Barbier.

**(Response 1)** Examiner respectfully disagrees with applicant, Barbier teaches this limitation as applicant has merely alleged without pointing to how the limitation is not taught by Barbier.

**(Argument 2)** Applicant has argued in Remarks Pg.7:

Independent claim 4 as amended recites a third reconfigurable interconnect stage - configurable to receive a second plurality of outputs of a second reconfigurable interconnect stage and to provide outputs back to inputs of clusters that include simulation engines. An example of this configuration is described in Applicant's specification, e.g., at p. 17, paragraph 52. The Office Action compares the third reconfigurable stage with crossbar 230 on the right side of Fig. 7 in Barbier, and the clusters of simulation engines with LE array 102 of Barbier. However, crossbar 230 on the right side of Fig. 7 does not provide outputs back to LE array 102. Thus, Barbier does not teach or suggest the third reconfigurable interconnect stage as now claimed. For at least this reason, it is submitted that amended claim 4 is allowable over Barbier.

**(Response 2)** As can be clearly seen the element 230 has a bidirectional arrow to the LE array further stating to-from LE array, thereby meeting the argued limitation.



Hence applicant's arguments are found to be unpersuasive. No new arguments are presented for dependent claims.

***FIGURE 7***

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**7. Claim 1-2, 4-10 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S.**

**Patent No. 5,907,697 issued to Barbier et al.**

Regarding Claim 1 (updated 7/28/08)

Barbier teaches a logic simulation system, a reconfigurable interconnect network comprising (Barbier: Fig.3 and associated disclosure): a plurality of groups of simulation processors having a plurality of outputs (Barbier: Fig3 & 4a and associated disclosure; Fig.10); for each of the groups of simulation processors a corresponding one of a plurality of a first reconfigurable interconnect stage having a plurality of inputs coupled to the outputs from the simulation processors, and further having a plurality of outputs (Barbier: Fig 6a & 10 at least and associated disclosure; Also see Fig.7 Element 114A & 114 B, element 230 on left – first reconfigurable interconnect stage; Fig.10 backplane assembly for each group of simulation processors on each board); for each of the first reconfigurable interconnect stages a corresponding one of a plurality of second reconfigurable interconnect stage coupled to a first subset of the outputs from the first reconfigurable interconnect stage (Barbier: Fig.7 Element 631; Elements 230 and 631 showing first and second interconnect stages for example), and further having plurality of outputs (Barbier:

Fig.7 Element 631 having outputs to Element 230 on left, 640 and 230 on right), wherein the first set of outputs from the second reconfigurable interconnect stage are coupled to first subset of the inputs of the first reconfigurable interconnect stage via plurality of feedback paths (Barbier: Fig.7 Element 631 path to 230 on the left); and a third reconfigurable interconnect stage having a plurality of inputs coupled to a second subset of the outputs from the second reconfigurable interconnect stage (Barbier: Fig.7 Element 230 on right of Element 631 as third reconfigurable interconnect) wherein the plurality of feedback paths each couples one of the outputs of the second reconfigurable interconnect stage to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage (Barbier: Fig.7) as seen feedback from second reconfigurable interconnect (Barbier: Fig.7 element 631) to first reconfigurable interconnect (Barbier: Fig.7 Element 230 on the left) is direct and does not pass through third reconfigurable interconnect (Barbier: Fig.7 Element 230 on the right).

Regarding Claim 2 (updated 7/28/08)

Barbier teaches wherein a second subset of the outputs from each of the first reconfigurable interconnect stage are coupled to inputs of the corresponding group of simulation processors (Barbier: Fig.3 & 4) as element 114a/b and 104 making up the first reconfigurable interconnect stage for simulation processor (element 102) and part of the first reconfigurable interconnect (element 104) providing out of first reconfigurable interconnect as feedback to the simulation processor (element 102).

Regarding Claim 4

Barbier teaches a logic simulation system (Barbier: Fig.1 and associated disclosure), a reconfigurable interconnect network (Barbier: Fig.3 & 4a and associated disclosure) a plurality of clusters, each cluster including plurality of simulation processors (Barbier: Fig.3, Fig.6a and Fig.10). Claim 4 further discloses similar limitations as claim 1 and is rejected for the same reasons.

Regarding Claim 5

Claim 5 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 6

Claim 6 has similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 7

Claim 7 has similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 8 (Updated 7/28/08 similarly to claim 1)

Claim 8 is identical to claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 9

Barbier teaches outputs of the second reconfigurable interconnect stage are coupled to the inputs of the third reconfigurable interconnect stage using a butterfly topology (Barbier: Fig.7).

Regarding Claim 10 (updated 7/28/08)

Barbier teaches each of the second and third reconfigurable interconnect stages comprises a crossbar (Barbier: Fig.3, 4a; 6b).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

- 8. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,907,697 issued to Barbier et al, in view of common knowledge of one skilled in the art.**

Regarding Claim 3

Barbier teaches including a memory coupled to the first & third reconfigurable interconnect stage as memory (Barbier: Fig.3 element 112; & Fig.7 has mirror of first reconfigurable interconnect stage as third reconfigurable interconnect stage) coupled to part of the first reconfigurable interconnect stage (Barbier: Fig.3 element



104) where first reconfigurable interconnect stage being dynamically configured in accordance with a content of the memory.

Barbier does not teaches explicitly including a memory coupled to the second reconfigurable interconnect stage.

It would be obvious to one skilled in the art to have memory attached to the second reconfigurable interconnect stage as well as because *firstly* - second reconfigurable interconnect stage has more connections for routing (Barbier: Fig.7 element 631), secondly – having the memory provides enhanced emulation capabilities (Barbier: Col.4 Lines 57-Col.5 Lines14).

### ***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for

proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

### ***Communication***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akash Saxena/  
Examiner, Art Unit 2128

/Alexander J Kosowski/  
Primary Examiner, Art Unit 2128